

This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

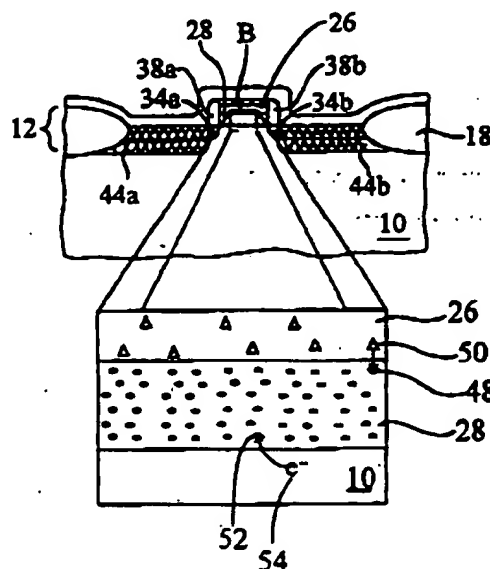
**As rescanning documents *will not* correct images,
please do not report the images to the
Image Problem Mailbox.**

PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6: H01L 21/314, 21/28	A1	(11) International Publication Number: WO 96/39713 (43) International Publication Date: 12 December 1996 (12.12.96)
(21) International Application Number: PCT/US96/09216 (22) International Filing Date: 6 June 1996 (06.06.96) (30) Priority Data: 08/470,321 6 June 1995 (06.06.95) US (71) Applicant: ADVANCED MICRO DEVICES, INC. [US/US]; Mail Stop 562, 5204 East Ben White Boulevard, Austin, TX 78741 (US). (72) Inventors: WRISTERS, Dirk, J.; 1904 Terisa Cove, Austin, TX 78728 (US); FULFORD, H. Jim; 9808 Woodshire Drive, Austin, TX 78748 (US); KWONG, Don, L.; 12031 Lincolnshire Drive, Austin, TX 78758 (US). (74) Agent: DRAKE, Paul, S.; Advanced Micro Devices, Inc., Mail Stop 562, 5204 East Ben White Boulevard, Austin, TX 78741 (US).	(81) Designated State: DE Published <i>With international search report.</i>	
(54) Title: A METHOD OF FORMING HIGH PRESSURE SILICON OXYNITRIDE (OXYNITRIDE) GATE DIELECTRICS FOR METAL OXIDE SEMICONDUCTOR (MOS) DEVICES WITH P+ POLYCRYSTALLINE SILICON (POLYSILICON) GATE ELECTRODES		
(57) Abstract <p>A silicon oxynitride (oxynitride) dielectric layer is presented using a process in which nitrogen is incorporated into the dielectric as it is grown upon a silicon substrate. The oxynitride layer is grown at elevated temperature and pressure in an ambient containing N_2O and/or NO. An MOS gate dielectric is advantageously formed from the oxynitride dielectric layer with a sufficient nitrogen concentration near the interface between a boron-doped polysilicon gate electrode and the gate dielectric as to prevent boron atoms from penetrating into the gate dielectric. Further, the oxynitride layer contains a sufficient nitrogen concentration near the interface between the gate dielectric and a silicon substrate as to reduce the number of high-energy electrons injected into the gate dielectric which become trapped in the gate dielectric. Nitrogen atoms in the gate dielectric near the interface between the boron-doped polysilicon gate electrode and the gate dielectric physically block boron atoms, preventing them from penetrating into the gate dielectric. Nitrogen atoms and silicon atoms form strong Si-N bonds at the interface between the gate dielectric and the silicon substrate, helping ensure injected electrons are not easily trapped in the oxynitride dielectric layer.</p>		



WO 96/39713

PCT/US96/09216

TITLE: A METHOD OF FORMING HIGH PRESSURE SILICON OXYNITRIDE (OXYNITRIDE) GATE DIELECTRICS FOR METAL OXIDE SEMICONDUCTOR (MOS) DEVICES WITH P+ POLYCRYSTALLINE SILICON (POLYSILICON) GATE ELECTRODES

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to the fabrication of an integrated circuit and more particularly the fabrication of metal oxide semiconductor (MOS) devices with p+ polycrystalline silicon (polysilicon) gate electrodes.

2. Description of the Relevant Art

A metal oxide semiconductor (MOS) transistor is a majority-carrier device in which current flow in a conducting channel formed between a source region and a drain region is modulated by an electrical potential (i.e., voltage) formed between a gate electrode and the substrate. A voltage formed between the gate electrode and the substrate which increases the number of majority carriers drawn into the channel region directly under the gate electrode results in an increase in the conductivity of the channel region. In order to draw majority carriers into the channel region, the voltage formed between the gate electrode and the substrate must exceed a certain threshold voltage level. This threshold voltage level depends on a number of factors including the gate electrode material, the gate insulator material, the thickness of the gate insulator, and the doping concentration in the channel region.

The threshold voltage levels of MOS transistors employed in a digital integrated circuit influence many characteristics of the circuit including maximum operating speed, power dissipation, and noise immunity. Lowering the threshold voltage level of an MOS transistor increases its current-driving capability. Employing MOS transistors with increased current-driving capability can increase the speed of logic level transitions. Lower threshold voltage levels are thus desirable for high-speed digital circuits.

As the threshold voltage level of an MOS transistor is lowered, however, the amount of subthreshold current flowing through the transistor may also increase. Subthreshold current is the current flowing from the source to the drain when the voltage between the gate electrode and the substrate is less than the threshold voltage level. This may be an important consideration in applications requiring low power dissipation and in large circuits with many MOS transistors. Noise immunities of circuits employing MOS transistors typically decrease when threshold voltage levels are reduced. This problem is exacerbated in circuits operable in high noise environments. Thus threshold voltage levels are often determined with consideration given to operating speed, power dissipation, and noise immunity. In general, threshold voltage levels of MOS transistors are lowered as much as the design application will allow.

In complementary MOS (CMOS) circuits, n-channel MOS transistors typically sink load current and p-channel MOS transistors typically source current to the load. Since it is desirable to be able to both charge and

WO 96/39713

PCT/US96/09216

discharge capacitive loads quickly, the threshold voltage levels of n-channel and p-channel MOS transistors are often reduced as much as possible.

As mentioned above, the threshold voltage level of an MOS transistor depends on a number of factors including the gate electrode material, the gate insulator material, the thickness of the gate insulator, and the doping concentration in the channel region. In order to reduce the threshold voltage level of an MOS transistor, a gate electrode material may be chosen such that the value of the work function of the gate electrode material is as close to the value of the work function of the substrate as possible. The gate electrode material and thickness of the underlying gate insulator may be selected such that the electrical capacitance between the gate electrode and the substrate is as high as possible.

Heavily doped polysilicon is typically used as a gate electrode in common self-aligned MOS processes. It adheres well to gate oxides (i.e., gate insulators), and is able to withstand the environments created during subsequent self-aligned processing steps. The work-function of n+ polysilicon is ideal for n-channel MOS transistors of CMOS circuits. Using n+ polysilicon gate electrodes, n-channel MOS transistors may be produced with threshold voltages of less than +0.7 volts for easily producible values of channel doping concentration levels and gate oxide thickness.

When the same n+ polysilicon is used for the gate electrodes of p-channel MOS transistors, however, the magnitudes of the resulting threshold voltage levels are well above 0.7 volts. In CMOS circuits, such p-channel devices would have less current driving ability than their n-channel complements. In order to reduce the magnitudes of the threshold voltage levels of p-channel MOS transistors, shallow implants of boron are commonly placed in the channel regions just under the gate electrodes of p-channel MOS transistors. The slightly p-type surfaces of the channel regions result in threshold voltage levels of reduced magnitude. However, such buried-channel devices are more susceptible to the punchthrough effect. As will be described below, the susceptibility of buried-channel devices to the punchthrough effect increases as device dimensions shrink.

Punchthrough occurs when the voltage formed between the gate electrode and the substrate is less than the threshold voltage level, and the reverse bias voltage on the drain region is large enough that the drain depletion region meets the source depletion region in the subsurface region below the gate electrode. When punchthrough occurs, majority carriers flow from the source region to the drain region, creating a subsurface flow of (subthreshold) current. Small MOS transistors with short channel lengths between the source and drain regions are particularly susceptible to the punchthrough effect. The use of boron to adjust threshold voltage levels of p-channel MOS transistors becomes less feasible as thinner gate insulators are used, due to the fact that larger doses of boron are required. As the active channel region is forced deeper into the substrate, the punchthrough problem worsens.

Another way to lower the magnitudes of threshold voltage levels of p-channel MOS devices is to use p-polysilicon for the gate electrodes of p-channel devices. P-type boron may be introduced into the polysilicon of the

WO 96/39713

PCT/US96/09216

See. Bhat et al., "Electrical Properties and Reliability of MOSFET's with Rapid Thermal NO-Nitrided SiO₂ Gate Dielectrics," IEEE Transactions on Electron Devices, Vol. 42 No. 5, May, 1995, pp. 907-914.

Incorporation of nitrogen into a pre-existing oxide (i.e., thermal nitridation) generally uses two types of source gases: 1) those comprising ammonia (NH₃), and 2) those comprising nitrous oxide (N₂O) and/or nitric oxide (NO). Thermally-nitrided oxides having high nitrogen concentrations at the surface and at the Si/SiO₂ interface may be formed using NH₃. See, Hori et al., "Ultra-Thin Re-Oxidized Nitrided-Oxides Prepared By Rapid Thermal Processing," IEDM Tech. Digest, 1987, pp. 570-573. A high nitrogen concentration at the surface of a such a thermally-nitrided oxide may provide a diffusion barrier to boron atoms, and a high concentration of nitrogen atoms at the Si/SiO₂ interface may increase the resistance of the dielectric to hot-carrier effects as described above.

Thermal nitridation using NH₃ cannot be accomplished without unavoidably introducing hydrogen atoms into the gate dielectric, however. It is well known that hydrogen atoms easily diffuse to the Si/SiO₂ interface and form weak Si-H bonds. These weak Si-H bonds are readily broken by hot electrons injected into the gate dielectric, forming empty electron states (or traps) which may be filled by the injected electrons. Trapped electrons contribute to the fixed oxide charge of the dielectric, causing a shift in the threshold voltage level. The number of trapped electrons increases with time, degrading device performance until device performance becomes unacceptable.

The deleterious effects of hydrogen incorporated into thermally-nitrided oxides produced using NH₃ may be reduced by re-oxidizing the thermally-nitrided oxides at high temperatures in an oxygen ambient. In this process, however, the nitrogen concentration near the surface of the thermally-nitrided oxides is reduced, while the nitrogen concentration near the Si-SiO₂ interface does not change appreciably. See, Hori et al., "Ultra-Thin Re-Oxidized Nitrided-Oxides Prepared By Rapid Thermal Processing," IEDM Tech. Digest, 1987, pp. 570-573. Unfortunately, the resulting nitrogen concentrations near the surface of re-oxidized nitrided oxides may not be sufficient to block boron penetration into the gate dielectrics. In addition, the required multiple high-temperature cycles (i.e., oxidation and nitridation) are undesirable for submicron MOS device fabrication processes.

It is postulated that processes employing thermal nitridation of pre-existing oxides or growth of oxynitrides using N₂O and/or NO at pressures of 1.0 atmosphere and below cannot achieve a sufficient nitrogen concentration at an upper surface (near an interface between a boron-doped polysilicon gate electrode and the gate dielectric) as to prevent boron atoms in the polysilicon gate electrode from penetrating into the gate dielectric.

It would thus be advantageous to have a method of forming a silicon oxynitride gate dielectric for p-type MOS devices at a pressure greater than 1.0 atmospheres which: 1) does not use a hydrogen-bearing source gas such as NH₃, 2) results in a dielectric with a sufficient concentration of nitrogen atoms at an upper surface (near an interface between a boron-doped polysilicon gate electrode and the gate dielectric) as to prevent boron atoms in the polysilicon gate electrode from penetrating into the gate dielectric, 3) results in a dielectric with a sufficient concentration of nitrogen atoms at a lower surface (near an interface between the gate dielectric and a silicon

WO 96/39713

PCT/US96/09216

substrate) as to reduce the number of high-energy electrons (i.e., hot electrons) injected into and thereafter trapped within the gate dielectric, and 4) avoids the added steps and high-temperature cycles associated with the thermal nitridation of a pre-existing oxide.

5

SUMMARY OF THE INVENTION

The problems outlined above are in large part solved by a method of forming high pressure silicon oxynitride (oxynitride) gate dielectrics for metal oxide semiconductor (MOS) devices with p+ polycrystalline silicon (polysilicon) gate electrodes. Using a high pressure thermal growth process, the method of the present invention produces an oxynitride dielectric layer in an ambient including N₂O and/or NO. An MOS gate dielectric, positioned between a boron-doped polysilicon gate electrode and a silicon substrate, is advantageously formed from such an oxynitride dielectric layer.

15 An MOS gate dielectric formed from an oxynitride dielectric layer has the following advantages. First, the oxynitride dielectric layer has a sufficient concentration of nitrogen atoms near the interface between the boron-doped polysilicon gate electrode and the gate dielectric as to prevent boron atoms in the boron-doped polysilicon gate electrode from penetrating into the gate dielectric. Second, the oxynitride dielectric layer has a sufficient concentration of nitrogen atoms near the interface between the gate dielectric and the silicon substrate as to reduce the number of hot electrons injected into and thereafter trapped within the gate. Nitrogen atoms at the polysilicon gate-oxynitride dielectric interface physically block boron atoms, preventing boron atoms in the boron-doped polysilicon gate electrode from penetrating into the gate dielectric. Nitrogen atoms present at the oxynitride dielectric-substrate interface form strong Si-N bonds, helping ensure injected hot electrons are not easily trapped in the gate dielectric.

25

Processes employing thermal nitridation of pre-existing oxides or growth of oxynitrides using N₂O and/or NO at pressures of 1.0 atmosphere and below cannot achieve a sufficient nitrogen concentration at an upper surface (near an interface between a boron-doped polysilicon gate electrode and the gate dielectric) as to prevent boron atoms in the polysilicon gate electrode from penetrating into the gate dielectric. It is postulated that the concentration of nitrogen atoms at the upper surface of an oxynitride gate dielectric must be at least 1.0×10^{21} atoms/cm³ in order to prevent boron atoms in the polysilicon gate electrode from penetrating into the gate dielectric.

30

Broadly speaking, the present oxynitride layer may be thermally grown by inserting a silicon substrate into a chamber containing a nitrogen-bearing gas such as N₂O, NO, or a combination of both N₂O and NO. The temperature and pressure within the chamber may then be increased. An oxynitride layer may thus be thermally grown at temperatures between 650EC and 900EC and at pressures from 2.0×10^5 Pa to 25.0×10^5 Pa (about 2.0 to 25.0 atmospheres). The resulting oxynitride layer may be patterned to form an MOS gate dielectric. The

35

WO 96/39713

PCT/US96/09216

concentration of nitrogen atoms in the gate dielectric formed from the oxynitride layer may be fairly constant, and sufficient to achieve the benefits described above.

5

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and advantages of the invention will become apparent upon reading the following detailed description and upon reference to the accompanying drawings in which:

10

Figure 1 is a partial cross-sectional view of a silicon substrate having a silicon nitride layer deposited over a pad oxide layer, all of which are formed over an active device region between field oxide layer openings on a frontside surface of the silicon substrate;

15 removed;

Figure 2 shows the silicon substrate of Figure 1 after the silicon nitride and pad oxide layers have been

Figure 3 shows the silicon substrate of Figure 2 after a silicon oxynitride (oxynitride) layer has been thermally grown over the frontside surface;

20

Figure 4 is a detailed view along plane A of Figure 3, illustrative of a substantially constant concentration of nitrogen atoms in the oxynitride layer;

25

Figure 5 is a graph of atomic concentrations of oxygen (O), nitrogen (N), and silicon (Si) versus depth along a profile of a first oxynitride layer grown according to the method of the present invention;

Figure 6 is a graph of atomic concentrations of oxygen (O), nitrogen (N), and silicon (Si) versus depth along a profile of a second oxynitride layer grown according to the method of the present invention;

30

Figure 7 shows the silicon substrate of Figure 3 after a polysilicon layer has been deposited over the oxynitride layer;

Figure 8 shows the silicon substrate of Figure 7 after the polysilicon layer and the oxynitride layer have been patterned to form a polysilicon gate electrode and a gate dielectric, respectively;

35

Figure 9 shows the frontside surface of the silicon substrate of Figure 8 being subjected to a relatively low concentration of p-type boron ions;

WO 96/39713

PCT/US96/09216

Figure 10 shows the silicon substrate of Figure 9 after an oxide layer has been formed over the frontside surface;

Figure 11 shows the silicon substrate of Figure 10 after a majority of the oxide layer over the frontside surface has been etched away, leaving oxide sidewall spacers adjacent to the polysilicon gate electrode and the gate dielectric;

Figure 12 shows the silicon substrate of Figure 11 being subjected to a relatively high concentration of p-type boron ions;

Figure 13 shows the silicon substrate of Figure 12 after a passivation layer has been formed over the entire frontside surface; and

Figure 14 is a detailed view along plane B of Figure 13, illustrative of a substantially constant concentration of nitrogen atoms in the gate dielectric used for blockage of boron atoms and/or trapping of hot electrons.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed, but on the contrary, the intention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the present invention as defined by the appended claims.

DETAILED DESCRIPTION OF THE INVENTION

Figures 1-14 will be used to describe how a p-type lightly doped drain (LDD) MOS transistor with an oxynitride gate dielectric may be formed on and in a frontside surface of a silicon substrate. In Figure 1, active device and field regions have been defined. A silicon nitride layer 14 on a pad oxide layer 16 remain over an active device region of a frontside surface 12 of a silicon substrate 10. A field oxide layer 18 has been thermally grown over field regions absent oxygen-impermeable silicon nitride layer 14 according to well-defined local oxidation of silicon (LOCOS) techniques.

Figure 2 shows silicon substrate 10 after silicon nitride layer 14 and pad oxide layer 16 have been removed from frontside surface 12. After field oxide layer 18 has been grown, silicon nitride layer 14 and pad oxide layer 16 are removed using, for example, a dry etch process or a wet chemical etch of known origin. A sacrificial oxide layer (not shown) may be grown and etched away from frontside surface 12 at this time, depending upon process constraints. The purpose of such a sacrificial oxide layer is to remove any residual nitride.

WO 96/39713

PCT/US96/09216

Figure 3 shows silicon substrate 10 after a silicon oxynitride (oxynitride) layer 20 has been thermally grown over frontside surface 12. Oxynitride layer 20 is grown under elevated temperature and pressure in a nitrogen-bearing ambient. Oxynitride layer 20 is thermally grown by placing silicon substrate 10 on-edge in a wafer boat, and inserting the wafer boat into an oxidation furnace set into a high-pressure chamber. The oxidation furnace contains a nitrogen-bearing gas such as N_2O , NO , or a combination of both N_2O and NO . Oxynitride layer 20 may be thermally grown at temperatures between 650EC and 900EC and at pressures from 2.0×10^5 Pa to 10.0×10^5 Pa. As shown in Figure 4, the concentration of nitrogen atoms 22 in resulting oxynitride layer 20 is fairly uniform not only across the frontside surface, but, more importantly, throughout the cross-sectional plane (or profile) of oxynitride layer 20. It is postulated that pressure associated with the high pressure chamber makes it thermodynamically favorable for the formation of Si-N bonds in the bulk of oxynitride layer 20, as compared to just at the Si/SiO₂ interface as observed for the formation of oxynitride layers at pressures of 1.0 atmosphere and below. As will be discussed hereinbelow, atomic nitrogen forms bonds with silicon and oxygen at uniform intervals within the oxynitride structure. These regular bonds help occupy diffusion avenues normally taken by subsequently introduced boron species. Advantages in having a uniform distribution of nitrogen are manyfold, some of which are to control boron diffusion and hot electron trapping therein.

Figure 5 shows a secondary ion mass spectroscopy (SIMS) plot of atomic concentration of oxygen (O), nitrogen (N), and silicon (Si) of an oxynitride layer grown on a silicon substrate using the method of the present invention. Atomic concentrations are shown from an upper surface of the oxynitride layer (0.0 angstroms) to a depth which exceeds the thickness of the oxynitride layer (about 100 angstroms). This plot shows the concentration of oxygen atoms is highest near the surface of the oxynitride layer, decreases sharply near a lower surface of the oxynitride layer (i.e., at the dielectric-substrate interface), and continues to decrease with increasing depth into the silicon substrate. The concentration of silicon atoms in the oxynitride layer and in the silicon substrate is fairly uniform at about 7.0×10^{20} atoms/cm³. The concentration of nitrogen atoms is also fairly uniform in the oxynitride layer at about 1.0×10^{21} atoms/cm³, being slightly higher at the surface. The concentration of nitrogen atoms decreases sharply near the dielectric-substrate interface, stabilizing at a background concentration of about 1.5×10^{19} atoms/cm³ in the silicon substrate.

Figure 6 shows a secondary ion mass spectroscopy (SIMS) plot of atomic concentration of oxygen (O), nitrogen (N), and silicon (Si) versus depth from a surface of an oxynitride layer about 70 angstroms thick grown on a silicon substrate using the method of the present invention. As in Figure 5, the concentration of oxygen atoms is highest near the surface, decreases sharply near the dielectric-substrate interface, and continues to decrease with increasing depth into the silicon substrate. The concentration of silicon atoms in the oxynitride layer and in the silicon substrate is fairly uniform at about 1.0×10^{21} atoms/cm³. The concentration of nitrogen atoms is also fairly uniform in the oxynitride layer at about 3.0×10^{21} atoms/cm³. The concentration of nitrogen atoms decreases sharply near the dielectric-substrate interface, and continues to decrease with increasing depth into the silicon substrate.

WO 96/39713

PCT/US96/09216

Processes employing thermal nitridation of pre-existing oxides or growth of oxynitrides using N_2O and/or NO at pressures of 1.0 atmosphere and below cannot achieve a sufficient nitrogen concentration at an upper surface (near an interface between a boron-doped polysilicon gate electrode and the gate dielectric) as to prevent boron atoms in the polysilicon gate electrode from penetrating into the gate dielectric. It is postulated that the concentration of nitrogen atoms at the upper surface of an oxynitride gate dielectric must be at least 1.0×10^{21} atoms/cm³ in order to prevent boron atoms in the polysilicon gate electrode from penetrating into the gate dielectric.

Figure 7 shows silicon substrate 10 after a polysilicon layer 24 has been deposited over oxynitride layer 20 on frontside surface 12. Polysilicon layer 24 may be deposited using a chemical vapor deposition (CVD) process.

Figure 8 shows silicon substrate 10 after polysilicon layer 24 and oxynitride layer 20 have been selectively etched to form polysilicon gate electrode 26 and gate dielectric 28, respectively. Polysilicon layer 24 and oxynitride layer 20 are patterned by masking the gate structures with polymerized photoresist and etching the exposed portions of polysilicon layer 24 and oxynitride layer 20.

Figure 9 shows silicon substrate 10 being subjected to a relatively low concentration of p-type boron ions 30. Boron ions penetrate into polysilicon gate electrode 26, forming a lightly-doped boron region 32. Using the well-known self-aligned technique, boron ions also penetrate into silicon substrate 10 at frontside surface 12, forming lightly-doped source-drain regions 34a and 34b. Silicon substrate 10 may be subjected to p-type boron ions using a diffusion or ion implantation process.

Figure 10 shows silicon substrate 10 after an oxide layer 36 has been formed over frontside surface 12. Oxide layer 36 may be deposited using various CVD techniques.

Figure 11 shows silicon substrate 10 after a majority of oxide layer 36 has been etched away, leaving only oxide sidewall spacers 38a and 38b adjacent to polysilicon gate electrode 26 and gate dielectric 28. Oxide layer 36 may be etched using a directional dry etch process.

Figure 12 shows silicon substrate 10 being subjected to a relatively high concentration of p-type boron ions 40. Boron ions penetrate into polysilicon gate electrode 26, forming a heavily-doped boron region 42. Boron ions also penetrate into silicon substrate 10 at frontside surface 12, forming heavily-doped source-drain regions 44a and 44b. Oxide sidewall spacers 38a and 38b prevent boron atoms from penetrating into silicon substrate 10 in the regions directly under oxide sidewall spacers 38a and 38b. Silicon substrate 10 may be subjected to p-type boron ions using a diffusion or ion implantation process.

Figure 13 shows silicon substrate 10 after a passivation layer 46 has been formed over the entire frontside surface 12 of silicon substrate 10 to seal out contaminants and moisture. The passivation layer is preferably a

WO 96/39713

PCT/US96/09216

doping said polysilicon gate electrode and source-drain regions of the silicon substrate surrounding the polysilicon gate electrode and gate dielectric with boron atoms.

8. The method as recited in claim 7, wherein the nitrogen-bearing ambient comprises nitrous oxide (N_2O).

9. The method as recited in claim 7, wherein the nitrogen-bearing ambient comprises nitric oxide (NO).

10. The method as recited in claim 7, wherein the nitrogen-bearing ambient comprises both nitrous oxide (N_2O) and nitric oxide (NO).

11. The method as recited in claim 7, further comprising increasing the temperature within said chamber about the silicon substrate to a level between 650EC and 900EC prior to placing the silicon substrate into the chamber.

12. The method as recited in claim 7, wherein said oxygen- and nitrogen-bearing ambient is substantially void of hydrogen atoms.

13. The method as recited in claim 7, further comprising growing a dielectric layer having a peak concentration of nitrogen atoms incorporated within said dielectric at an elevational level near an upper surface of said dielectric proximate to said polysilicon layer.

14. The method as recited in claim 7, further comprising growing a dielectric layer having a peak concentration of nitrogen atoms incorporated within said dielectric at an elevational level near a lower surface of said dielectric proximate to said silicon substrate.

15. The method as recited in claim 7, further comprising growing a dielectric layer having a peak concentration of nitrogen atoms incorporated within said dielectric at an elevational level near an upper surface and a lower surface of said dielectric proximate to said polysilicon layer and silicon substrate, respectively.

16. The method as recited in claim 7, wherein the pressure within said chamber about the silicon substrate is increased to a level between 2.0 atmospheres and 25.0 atmospheres.

17. The method as recited in claim 7, wherein the concentration of nitrogen atoms within said gate dielectric near the interface between the polysilicon gate electrode and the gate dielectric is sufficient to prevent boron atoms in the polysilicon gate electrode from penetrating into the gate dielectric.

18. The method as recited in claim 7, wherein the concentration of nitrogen atoms within said gate dielectric near the interface between the gate dielectric and the silicon substrate is sufficient to reduce the number of high-

WO 96/39713

PCT/US96/09216

energy electrons injected into the gate dielectric from the silicon substrate which become trapped in the gate dielectric.

19. A method of forming a gate dielectric having enhanced dielectric capacity, comprising:

growing an oxynitride film upon an exposed surface of a silicon substrate, wherein oxygen and nitrogen atomic species are uniformly distributed throughout a cross-sectional profile of said film;

depositing a polysilicon film upon said oxynitride film;

patternning said polysilicon film and said oxynitride film using a sequential etch process to form a polysilicon gate electrode aligned with a underlying gate dielectric; and

exposing the upper and lower surfaces of said gate dielectric to boron atoms originating from respective said polysilicon film and silicon substrate, wherein said nitrogen atomic species within the gate dielectric substantially repels boron atoms from diffusing or injecting therein.

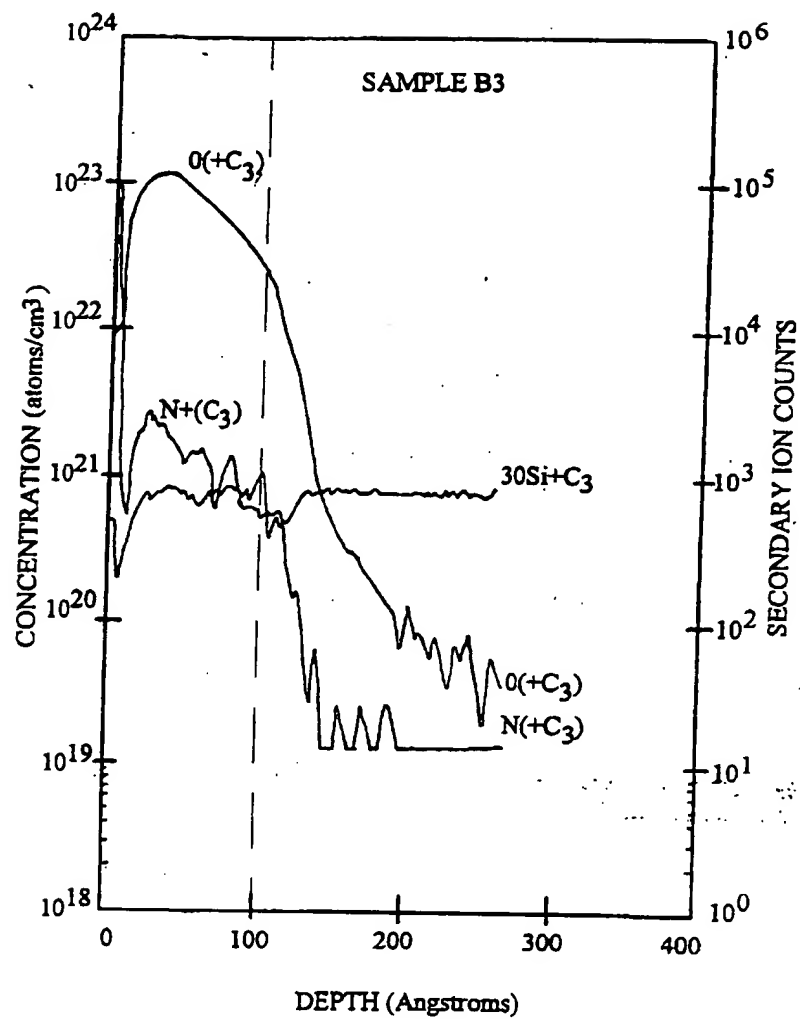


Fig. 5

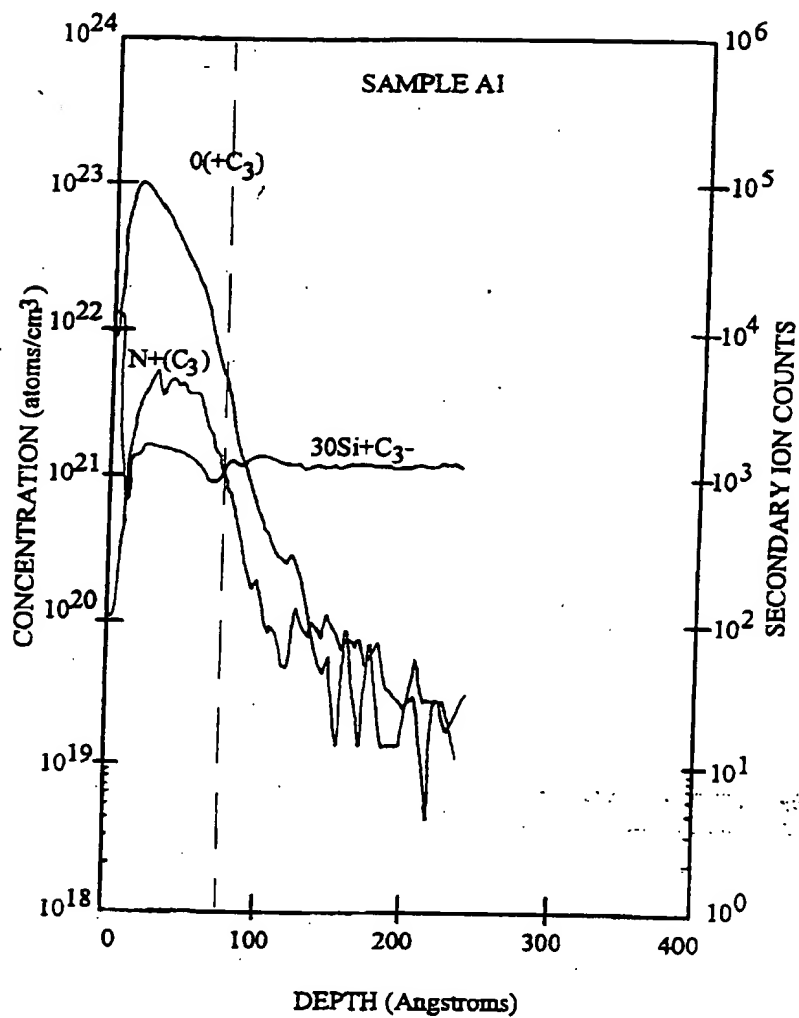
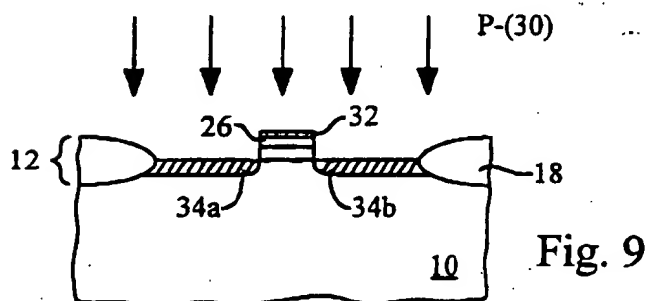
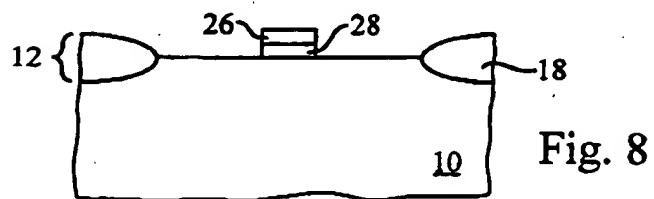
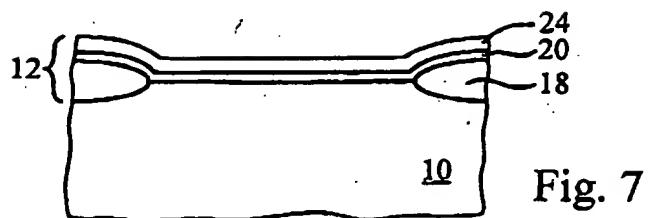


Fig. 6



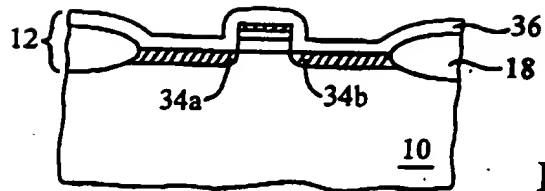


Fig. 10

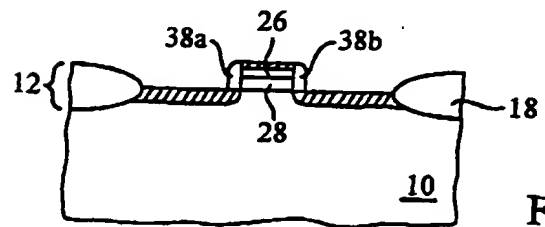


Fig. 11

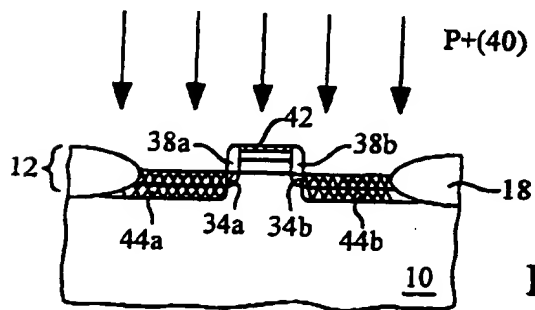
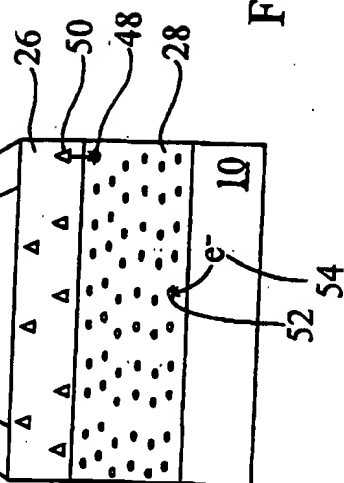
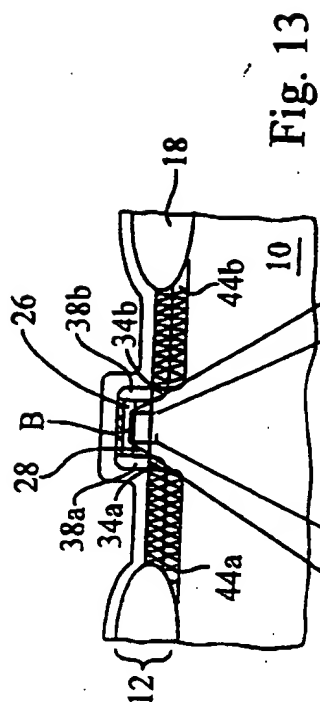


Fig. 12



INTERNATIONAL SEARCH REPORT

 Int. Patent Application No.
 PCT/US 96/09216

 A. CLASSIFICATION OF SUBJECT MATTER
 IPC 6 H01L21/314 H01L21/28

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 H01L

Documentation searched other than minimum documentation is the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US,A,5 397 720 (KWONG DIM-LEE ET AL) 14 March 1995 see column 3-4; figures 1,2	19
X	IEEE TRANSACTIONS ON ELECTRON DEVICES, vol. 41, no. 4, 1 April 1994, pages 546-552, XP000442972 HISAYO SASAKI MOMOSE ET AL: "ELECTRICAL CHARACTERISTICS OF RAPID THERMAL NITRIDED-OXIDE GATE N- AND P-MOSFET'S WITH LESS THAN 1 ATOM% NITROGEN CONCENTRATION" see page 546, paragraph 1 - page 547, paragraph 5	19
	--- -/--	

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents:

- *A* document defining the general state of the art which is not considered to be of particular relevance
- *E* earlier document but published on or after the international filing date
- *L* documents which may throw doubts on priority claim(s) or which is cited to establish the publication date of another claim or other typical reason (as specified)
- *O* document referring to an oral disclosure, use, exhibition or other means
- *P* documents published prior to the international filing date but later than the priority date claimed

- *T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principles or theory underlying the invention
- *X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- *Y* documents of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is considered with one or more other such documents, such combinations being obvious to a person skilled in the art.
- *A* document member of the same patent family

Date of the actual completion of the international search

27 August 1996

Date of mailing of the international search report

13. 09. 96

Name and mailing address of the ISA

 European Patent Office, P.O. Box 518, 8001 Zurich
 NL - 2280 HV Rijswijk
 Tel. (+31-70) 340-2040, Telex 31 451 epo nl,
 Fax (+31-70) 340-2016

Authorized officer

Hammett, E

INTERNATIONAL SEARCH REPORT

C/(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		Int. Appl. No. PCT/US 96/09216
Category	Citation of documents, with indication, where appropriate, of the relevant passages	Relevant to class No.
A	<p>APPLIED PHYSICS LETTERS, vol. 61, no. 26, 28 December 1992, pages 3163-3165, XP000334715 YOSHIO OKADA ET AL: "Oxinitride gate electrics prepared by rapid thermal processing using mixtures of nitrous oxide and oxygen" see page 3163 - page 3164</p>	1-18
A	<p>APPLIED PHYSICS LETTERS, vol. 57, no. 18, 3 September 1990, pages 1810-1811, XP000164507 HYUNSANG HWANG ET AL: "ELECTRICAL CHARACTERISTICS OF ULTRATHIN OXYNITRIDE GATE DIELECTRIC PREPARED BY RAPID THERMAL OXIDATION OF Si IN N₂O" see page 1810</p>	1-18

WO 96/39713

PCT/US96/09216

1/6

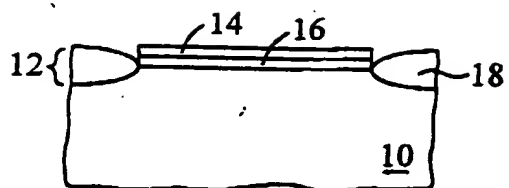


Fig. 1



Fig. 2

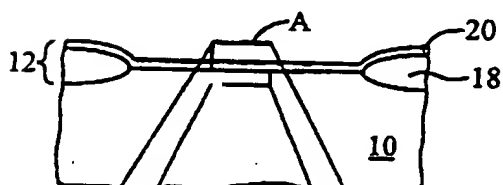


Fig. 3

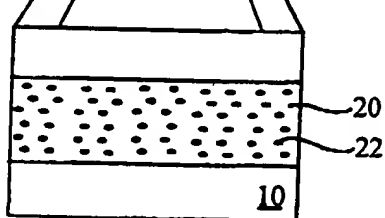


Fig. 4

INTERNATIONAL SEARCH REPORT

Information on patent family members

Int. Application No.

PCT/US 96/09216

Patent documents
cited in search reportPublication
datePatent family
member(s)Publication
date

US-A-5397720

14-03-95

US-A-

5541436

30-07-96